ABSTRACT OF THE DISCLOSURE

It is an object to provide a semiconductor device having a buried multilayer wiring structure in which generation of a resolution defect of a resist pattern is suppressed and generation of a defective wiring caused by the resolution defect is reduced. After a via hole (7) reaching an etching stopper film (4) is formed, annealing is carried out at 300 to 400℃ with the via hole (7) opened. As an annealing method, it is possible to use both a method using a hot plate and a method using a heat treating furnace. In order to suppress an influence on a lower wiring (20) which has been manufactured, heating is carried out for a short time of approximately 5 to 10 minutes by using the hot plate. Consequently, a by-product staying in an interface of an upper protective film (6) and an interlayer dielectric film (5) having a low dielectric constant and a by-product staying in an interface of the etching stopper film (4) and the interlayer dielectric film (5) having a low dielectric constant are discharged so that an amount of the residual by-product can be decreased.